Novel LTCC-/BGA-Modules for Highly Integrated Millimeter-Wave Transceivers

Johann Heyen, Thomas v. Kerssenbrock*, Alexander Chernyakov*, Patric Heide*, and Arne F. Jacob

Institut für Hochfrequenztechnik, Technische Universität Braunschweig, P/O 3329, D-38023 Braunschweig, Germany; Email: j.heyen@tu-braunschweig.de

* EPCOS AG, Product Development Modules, Anzinger Straße 11, D-81617 Munich, Germany

Abstract **— This paper demonstrates advanced packaging concepts for highly integrated encapsulated millimeter-wave modules. Millimeter-wave monolithic integrated circuits (MMIC) are flip-chip mounted on top of a LTCC package (low temperature co-fired ceramic). This type of "smart package" can integrate all kinds of passive functions as well as compact interconnections between MMIC and vertical feedthroughs. The bottom side of this package is connected via standard ball grid array (BGA) to a low-cost laminate PCB serving as motherboard for multiple LTCC modules. Fabricated LTCC test structures and LTCC test packages provide good performance up to about 30GHz.**

I. Introduction

In order to make millimeter-wave electronics for commercial applications such as microwave radio or automotive radar a successful high-volume product, low-cost manufacturing, and high integration are essential. LTCC technology, nowadays widely used for frontend modules for price-sensitive applications like mobile phones [1, 2], is very well suited to meet these requirements. It offers a great potential for passive integration, and this even up to millimeter-wave frequencies, where so far almost exclusively thinfim alumina substrates have been used. Recent work on LTCC modules has demonstrated solutions for 5GHz Wireless-LAN [3, 4] and Ku-Band V-SAT [5] applications. These first generation transceiver modules leave further potential for much higher integration.

With continously improving LTCC production technologies [6] it is becoming feasible to realize fully integrated mm-wave modules with tiny size as small as a fingernail. Advanced packaging techniques, already used in mass production of chip-size SAW filters (surface acoustic wave) [7, 8] can be applied to these LTCC modules, such that a compact encapsulation with excellent hermetic sealing is obtained at very low cost. Furthermore, millimeter- wave transceivers can be split into functional blocks being realized as SMT-mountable submodules. A SMD-type package for a single 26.5GHz MMIC has already been presented in [9]. Because of the chosen single layer laminate passive drop-on components inside the package walls were still needed. The LTCC module approach being pursued in this paper offers much higher passive integration and more compact packaging opportunities for future miniaturized millimeter-wave transceiver modules.

II. Module Architecture

Fig. 1 illustrates the proposed module concept. The top and the bottom LTCC layers host the 1st and 2nd level interconnects, respectively. All necessary transitions between the MMIC or feedthroughs from the top to bottom layer are vertically integrated inside the LTCC. Hence, interference with the proposed hermetic encapsulation having a metal shielding in close proximity to the LTCC top surface is avoided. The inner space of the LTCC is allocated for passive functions like e.g. filters, couplers or RF block capacitors. The LTCC module is linked to the motherboard via the 2nd level interconnects, which consist of solder balls with standard BGA pitch dimensions of 500µm or 800µm. Further LTCC based modules can be connected on the low cost laminate and linked with each other via this standard BGA interface. Although the BGA provides an interconnection for low-frequency as well as mm-wave signals, micro BGAs (µBGA) as suggested in [3] are not required, thus a high-volume production technology can solely be used.

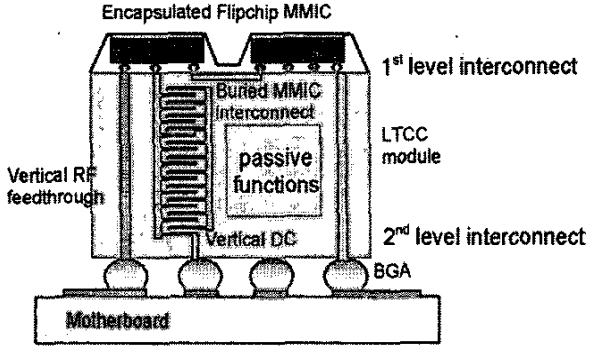

Fig. 1: LTCC Module.

0-7803-7695-1/03/$17.00 © 2003 IEEE

The following LTCC layer topology is considered for the designs described next. The substrate consists of 12 dielectric layers having a dielectric constant ε_r of 7.8 (K8). While the two outer layers are 38µm thick the remaining 10 inner layers are 55µm thick. 10µm thick conductors are printed in between the layers with minimum line width and spacing of 100µm. Vertical transitions are realized using vias of 100µm in diameter being interlinked on adjacent layers with catchpads of 200µm in diameter.

III. 3D-Integrated Passive Functions

Key components of such a LTCC module are the vertical feedthroughs. They connect the top surface of the LTCC hosting the active devices with the bottom side. There, input and output pads for the RF signals as well as DC and control signals are located. Especially the RF feedthrough is a design challenge because it must establish a proper millimeter-wave connection. Indeed, it leads the RF signal through multiple dielectric layers from the topside of the LTCC to its bottomside.

A. Vertical feedthroughs and transitions

The simplest possible feedthrough between a CPW on the top and the bottom LTCC layer can be realized by a vertical three-wire structure.

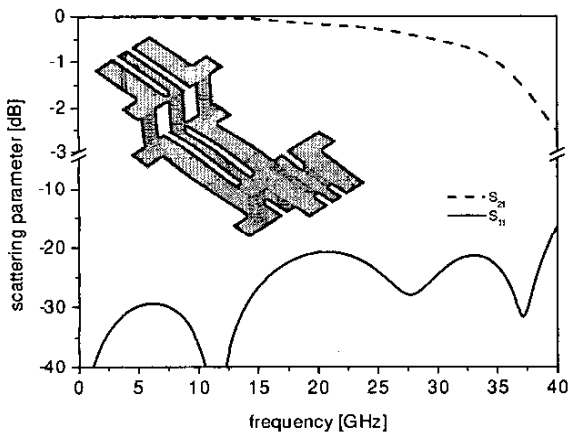

Fig. 2: Vertical three-wire transition.

Fig. 2 shows a corresponding back-to-back configuration with CPW feeding lines on the top layer. The simulated performance is shown for an optimum via pitch of 500µm for low input reflection (S_{11}<-20dB) and high transmission (S_{21}>-1dB) up to millimeter-waves. The overall area of such a CPW fed transition designed for the substrate described above is 1.2x0.2mm^2. Buried transitions between MMIC are not necessarily top to bottom interconnections. In order to leave as many layers as possible available for further passive integration of other structures such a buried chip-to-chip interconnect (BCCT) should ideally occupy only little space in vertical and lateral direction. Different configurations were considered to realize a 50Ω buried line. Triplates and striplines were found to be unqualified because of their overall size. Buried coplanar lines are therefore used for interconnections because they are very compact and have their fields concentrated around the slot. Therefore, good isolation between the interconnection and other adjacent, passive, integrated components is automatically given, thus, minimizing the occupied space.

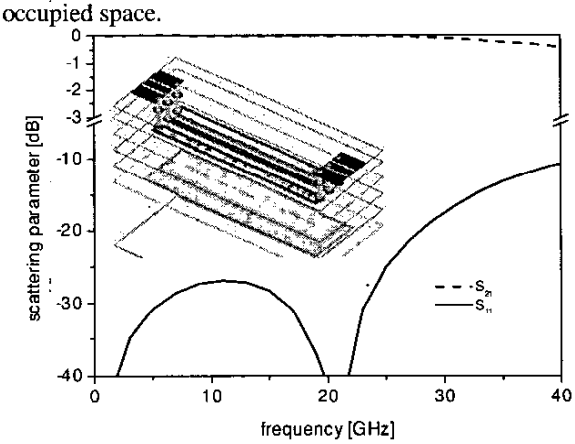

Fig. 3: Buried MMIC interconnection.

The buried CPW with additional ground plane depicted in Fig. 3 is vertically interconnected by vias to two 50Ω CPW feeding lines on top. The simulated input reflection S_{11} of this structure remains below -10dB up to 40GHz. For these transitions the overall vertical depth of 250µm maximum still offers reasonable space for passive integration below the shielding ground plane.

B. Embedded RF-block capacitors

In order to achieve an integrated DC supply with shunt RF-block capacitor, an interdigital arrangement of parallel plates as sketched in Fig.1 was evaluated.

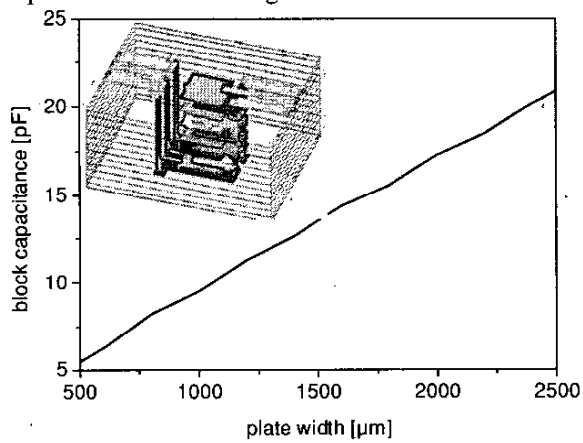

Fig. 4: RF-block test structure and extracted capacitance.

Such LTCC-integrated capacitors can replace chip capacitors, that have usually to be placed on top of the substrate. Fig. 4 shows the structure connected via a vertical three-wire structure and feed lines allowing two-port on-wafer analysis on the same layer. The plate length is set to 0.8mm while the width is varied. The corresponding extracted block capacitances are also shown in Fig. 4. Here, the maximum achievable capacitance is limited to a few pF by the number of layers and the low dielectric constant (K8) of the used LTCC substrate. However, using thinner layers and higher dielectric constant materials (K20, K80) for these RF blocking capacitors, much larger capacitance values can be achieved.

IV. Realized Test Modules and Packages

In order to experimentally evaluate the performance of our packaging and interconnection concepts, a low-noise amplifier (LNA) was packaged and several other test packages with various integrated passive functions and interconnects were fabricated using EPCOS' 8-inch commercial LTCC process.

A. LTCC Amplifier Module

Hittite's HMC263 MMIC LNA was used as the active device. LTCC modules were designed for both flip-chip and wire-bond assembly of the MMIC on top of the LTCC substrate. Fig. 5 shows the realized modules.

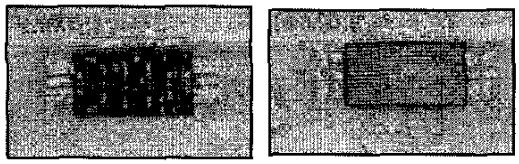

Fig. 5: Realized LTCC amplifier modules.

The center region below the MMIC of each layout is occupied by two RF blocks (refer to Fig. 4). Furthermore, CPW lines on the top layer in the outer left and right parts of the modules are visible. They are connected to the bottom layer by vertical three-wire structures as depicted in Fig. 2. Each module offers several pads for probing purposes on the top and bottom layer. For comparison reasons the same MMIC was measured in bare die configuration and via vertical interconnects. The changeover to another configuration was achieved by simply removing or adding wire-bonds on the top layer that bridged the corresponding feed lines. Fig. 6 shows the measured performance of a MMIC mounted in wire-bond technology for the following configurations. First, the bare MMIC mounted on top of the module was measured. Then, this MMIC was wire-bonded to the vertical interconnects for the RF signals and for the DC supply without shunt RF block capacitor. Finally, the DC supply bonds were rerouted to vertical DC supplies with integrated shunt capacitor. Connecting the MMIC via the various vertical interconnects does not degrade the chip performance. For all configurations the input reflection S_{11} is within the chip specification. In comparison to the bare MMIC, the transmission S_{21} is only slightly attenuated (worst case 2dB). This insertion loss corresponds to the transition losses expected from the two vertical three-wire transitions and further losses introduced by the wire-bonds.

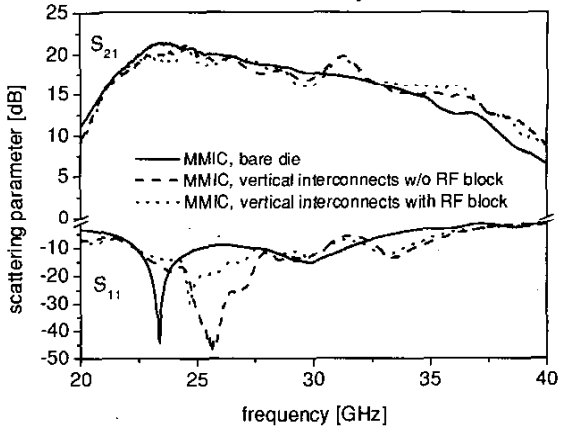

Fig. 6: Measured performance of LNA in different configurations.

B. LTCC BGA Package

Finally, test packages for verification of the 2nd level interconnects based on standard BGAs were realized. LTCC packages consisting of a CPW line on top vertically fed by two three-wire-structures at both ends were fabricated using two different designs. In the first design, the via pitch of the three-wire-structure was set to 500µm. For this value, the transmission characteristic of the vertical interconnect was found to be optimum. This value also correlates with the desired pitch for standard BGA. In the second design the optimum via pitch of 500µm was tapered to BGA pitch of 800µm within the lower LTCC layers. These LTCC packages were mounted on a low-cost laminate suitable for millimeter-wave applications. Here, Rogers' Ro4003 was chosen. The substrate with a dielectric constant ε_r=3.38 was 200µm thick. Both sides had 35µm thick copper cladding. In order to keep the overall size of transmission lines on Ro4003 small, microstrip lines (width=465µm) were preferred rather than CPW. Then, suitable transitions from the microstrip line to CPW were required for the 2nd level interconnects and for CPW probe launchers. Different CPW-to-microstrip transitions on Ro4003 were designed. The ground connection was achieved by quarter wave (radial) stubs, by 200µm filled vias or by a combination of both. When quarter wave stubs were involved they were designed for 26.5 GHz leading to a stub length of approx. 1800µm. Fig. 7 (a)

depicts such landing structures on Ro4003 before mounting the LTCC package. A resist mask is printed on the Ro4003 in order to limit the solder flow. It consists of circles with an outer and inner radius of 400µm and 150µm, respectively. Due to the local character of the solder resist mask its influence on the RF performance should be low as expected from simulations not shown here. Solder was applied to the vertical three-wire structure at the bottom side of the LTCC such that a ball with approx. 300µm diameter was attached to each vertical interconnect after heating. These LTCC packages were placed on the Ro4003 substrate such that each ball was surrounded by a solder resist circle. This arrangement was finally assembled in a reflow process.

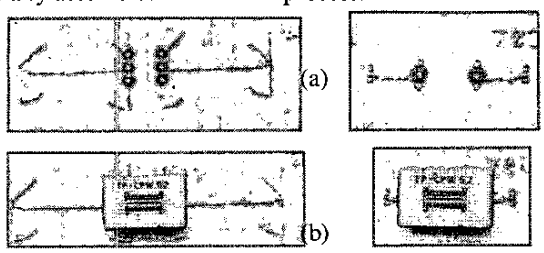

Fig. 7: LTCC test packages mounted on Ro4003 substrate using standard BGA technology.

Different LTCC test packages were mounted on various landing structures with a BGA pitch of 500µm and 800µm, respectively.

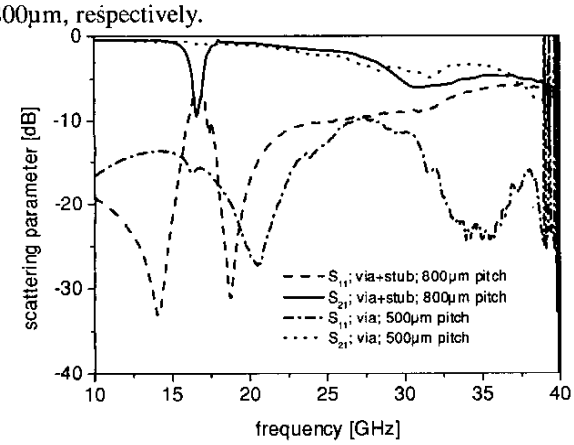

Fig. 8: Measured scattering parameters of 500µm and 800µm pitch BGA packages.

The 500µm BGA pitch packages are shown in Fig. 7 (b). Measurement results for both BGA pitches are depicted in Fig. 8. In all cases TRL calibrations were performed to eliminate the influence of the probe launchers. Due to the chosen calibration standards this could successfully be performed up to 38GHz. The resonance at 17GHz is due to the simultaneous use of quarter wave stubs and vias for the CPW-to-microstrip transitions. For the 500µm BGA pitch with two different CPW-to-microstrip transitions the input reflection S_{11} remains below -10dB. The overall transmission S_{21} is better than –2dB (–3dB) up to 27GHz (30GHz). This leads to low transmission loss of about 1dB per BGA transition. Also the measurements of the 800µm BGA pitch setups show good results up to 30GHz. This experimental study illustrates the feasibility of our packaging approach which is solely based on standard BGA and LTCC technologies.

V. Conclusion

LTCC-based package solutions for millimeter wave applications were presented. These modules can be mounted on a low cost laminate PCB using a standard BGA interface which has demonstrated good performance up to 30GHz. The functionality of this approach was fully validated by scattering parameter measurements performed on LTCC test modules assembled with commercial 26GHz LNA&MMIC. The LTCC modules were fabricated in a commercial 8-inch LTCC process at EPCOS.

References

[1] M. Hikita, N. Matsuura, K. Yokoyama, N. Shibagaki, L. Sakiyama: "SAW FEMs for GSM-Based Multi-Band Cellular Phones with Direct Conversion Demodulation", *IEEE MTT-S Int. Microwave Symp. Dig.*, Seattle, WA, June 2002, pp. 1483-1486.

[2] P. Hagn, A. Przadka, V. Gebhardt, U. Bauernschmitt: "Ceramics: The Platform for Duplexers and Frontend-Modules", *2002 IEEE Ultrasonics Symposium.*

[3] S. Pinel, S. Chakraborty, M. Roellig, R. Kunze, S. Mandal, H. Liang, C-H. Lee, R. Li, K. Lim, G. White, M. Tentzeris, and J. Laskar, "3D Integrated LTCC Module using µBGA technology for compact C-band RF Front-End Module," *IEEE MTT-S Int. Microwave Symp. Dig.*, Seattle, WA, June 2002, pp. 1553-1556.

[4] S. Yamanouchi, K. Haraguchi, K. Kunihiro, K. Ikuina, M. Fujii, H. Hida, "A 0.04 cc Power Amplifier Module with Fully Integrated Passives in a Hybrid LTCC Substrate for 5-GHz Wireless LANs," *32nd EUMC*, Milano, September 2002, pp. 465-468.

[5] C.-H. Lee, A. Sutono, S. Han, and J. Laskar, "A Compact LTCC Ku-band Transmitter Module with Integrated Filter for Satellite Communication Application," *IEEE MTT-S Int. Microwave Symp. Dig.*, Phoenix, AZ, May 2001, pp. 945-948.

[6] H. Flühr, C. Hoffmann, C. Block: "Advanced LTCC Front-End Modules and Processes for New Mobile Communication Standards", *2001 IEEE MTT-S Conference, Workshop Proceedings.*

[7] P. Selmeier, R. Grünwald, A. Przadka, H. Krüger, G. Feiertag, and C. Ruppel, "Recent Advances in SAW Packaging," *IEEE Ultrasonics Symp.*, 2001, pp. 283-292.

[8] C. Eder, G. Fischerauer, R. Thomas, P. Hagn, G. Riha: "SAW Filters for 3G Systems: A Quantum Leap in Size and Passive Integration is Ahead", *2001 IEEE Ultrasonics Symp.*

[9] K. Beilenhoff, P. Quentin, S. Tranchant, O. Vaudescal, M. Parisot, H. Dämbkes, "Full 26 GHz MMIC Chipset for Telecom Applications in SMD-Type Packages," *32nd EUMC*, Milano, September 2002, pp. 275-278.